REMARKS

The Office Action dated October 23, 2003, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1 and 9 have been amended. New claims 16 and 17 have been added. Applicant submits that the new claims as well as the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1-17 are pending in the present application and are respectfully submitted for consideration.

Claims 1-4, 6-12, 14 and 15 were rejected under 35 U.S.C. § 102(a) as being anticipated by the instant application's disclosed prior art (hereinafter "APA"). Applicant respectfully submits that each of claims 1-4, 6-12, 14 and 15 recites subject matter that is neither disclosed nor suggested by APA.

Claim 1 recites a signal processing circuit having a decision feedback equalizer for waveform-equalizing a digital signal in accordance with a clock signal and generating the waveform-equalized digital signal, and a timing recovery PLL, connected to the decision feedback equalizer, for generating the clock signal, the clock signal having a phase which is substantially coincident with the phase of the digital signal, based on the phase difference between the digital signal and the clock signal, and supplying the clock signal to the decision feedback equalizer. The decision feedback equalizer includes, a prefilter for filtering the digital signal and generating a filtered digital signal, a decision circuit, connected to the prefilter, for performing a calculation with a feedback signal and the filtered digital signal and generating a calculation signal,

and for analyzing the calculation signal in accordance with predetermined criteria to generate a decision signal, and a shift register, connected to the decision circuit, for sampling the decision signal in accordance with the clock signal and storing sampling data. The sampling data stored in the shift register is output from the shift register as the waveform-equalized digital signal. In addition, the decision feedback equalizer includes a feedback filter, connected to the shift register, for receiving the sampling data and generating the feedback signal using the sampling data, and a loop control circuit for calculating a phase difference between the filtered digital signal and the feedback signal and controlling a feedback loop formed by the decision circuit, the shift register, and the feedback filter based on the phase difference.

Claim 9 recites, in a signal processor, a feedback control method having the steps of filtering a digital signal to generate a filtered digital signal, performing a calculation with a feedback signal and the filtered digital signal to generate a calculation signal, and analyzing the calculation signal in accordance with predetermined criteria to generate a decision signal. In addition, the steps include sampling the decision signal in accordance with a clock signal to store sampling data in a shift register; generating the feedback signal using the sampling data stored in the shift register, and generating the clock signal, which is substantially coincident with the phase of the digital signal, based on a phase difference between the digital signal and the clock signal. Furthermore, the steps includes calculating a phase difference between the filtered digital signal and the feedback signal, and selecting whether the feedback signal is fed back to the step of generating the addition signal based on the phase difference.

Claim 15 recites in a signal processor, a feedback control method having the steps of filtering a digital signal to generate a filtered digital signal, adding a feedback signal and the filtered digital signal to generate the addition signal, analyzing the addition signal in accordance with predetermined criteria to generate a decision signal, sampling the decision signal in accordance with a clock signal to store sampling data in a shift register, generating the feedback signal using the sampling data stored in the shift register, and calculating a first phase difference between the digital signal and the clock signal using the decision signal and a first reference signal. The first reference signal has a first predetermined value at preset control point of the filtered digital signal. In addition, the steps include generating the clock signal having a phase which is substantially coincident with the phase of the digital signal, based on a first phase difference, determining whether the first phase difference is within a predetermined range, feeding back the feedback signal to the step of generating the addition signal when the first phase difference is within the predetermined range, calculating a second phase difference between the digital signal and the clock signal using the decision signal and a second reference signal, wherein the second reference signal has a second predetermined value at the preset control point preset of the decision signal, and regenerating the clock signal having a phase which is substantially coincident with the phase of the digital signal, based on the second phase difference.

Accordingly, at least one of the essential features of the present invention with respect to the present invention is "a loop control circuit for calculating a phase difference between the filtered digital signal and the feedback signal and controlling a feedback loop formed by the decision circuit, the shift register, and the feedback filter

based on the phase difference." As such, the present invention results in the advantage of having a signal processing circuit that prevents pseudo lock of the timing recovery PLL.

It is respectfully submitted that the prior art fails to disclose or suggest at least the combination of elements of the Applicant's invention as set forth in claims 1, 9 and 15, and therefore fails to provide the advantages which are provided by the present application.

APA discloses a signal processing circuit 10 including an analog-to-digital converter (ADC) 11, a decision feedback equalizer (DFE) 12, coefficient registers 13 and 14, a PLL phase error detection circuit 15, a timing recovery PLL (TR-PLL) 16, and a control circuit 17.

The ADC 11 samples an analog signal read from a recording medium in accordance with a clock signal CLK supplied from the TR-PLL 16 and converts the analog read signal to a digital read signal. The DFE 12 includes a forward (FW) filter 21, an adder 22, a comparator 23, a shift register 24, a feedback (FB) filter 25, an inverter circuit 26, and switches 27, 28, and 29.

Applicant respectfully submits that each and every element recited within claims 1, 9 and 15 is neither disclosed nor suggested by APA. In particular, Applicant submits that the signal processing circuit and the feedback control method as recited in the present application is clearly distinct from that which is disclosed in APA. Specifically, it is submitted that APA fails to disclose or suggest at least the following elements of the claimed invention.

Claim 1: "a loop control circuit for calculating a phase difference between the filtered digital signal and the feedback signal and controlling a feedback loop formed by the decision circuit, the shift register, and the feedback filter based on the phase difference."

Claim 9: "calculating a phase difference between the filtered digital signal and the feedback signal; and selecting whether the feedback signal is fed back to the step of generating the addition signal based on the phase difference."

Claim 15: "determining whether the first phase difference is within a predetermined range; feeding back the feedback signal to the step of generating the addition signal when the first phase difference is within the predetermined range."

As mentioned above, Figure 1 of APA merely discloses a control circuit 17 that controls a feedback loop based on data output from the shift register 24. In contrast, the present invention controls a feedback loop based on a phase difference between a digital signal and a feedback signal (claims 1 and 9). Furthermore, the present invention performs a feedback when a phase difference between a digital signal and a clock signal is within the predetermined range (claim 15). Accordingly, the Applicant submits that APA fails to disclose or suggest each and every element recited in claims 1, 9 and 15 of the present application, and therefore is allowable.

As for claims 2-4, 6-8, 10-12 and 14, it is submitted that each of these claims is dependent on independent claims 1 and 9, respectively. As such, each of claims 2-4, 6-8, 10-12 and 14 is allowable due to its dependency on allowable claims 1 and 9, respectively.

Claims 5 and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over APA, and further in view of Kobayashi et al. (U.S. Patent No. 5,963,581, "Kobayashi"). It is respectfully submitted that each of claims 5 and 13 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Applicant submits that claims 5 and 13 depend from allowable claims 1 and 9, respectively, and therefore these claims are likewise allowable.

As for new claims 16 and 17, it is respectfully submitted that each of new claims 16 and 17 recites subject matter that is neither disclosed nor suggested by the cited prior art.

In view of the above, Applicant respectfully submits that each of claims 1-17 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also submits that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1-17 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300 referencing Attorney Docket No. 108075-09006.

Respectfully submitted,
ARENT FOX PLLC

Sam Huang
Attorney for Applicant
Registration No. 48,430

Customer No. **004372**
1050 Connecticut Avenue, N.W., Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-4810

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Enclosures: RCE Transmittal
Petition for Extension of Time